

# CURRICULUM VITÆ

<b>NAME</b>	VIMAL KUMAR						
<b>FATHER'S / MOTHER'S NAME</b>	YOGENDRA SINGH / INDRAWATI DEVI						
<b>D.O.B</b>	15/07/1992						
<b>SEX</b>	MALE						
<b>MARITAL STATUS</b>	SINGLE						
<b>EDUCATIONAL QUALIFICATION</b>	<b>STANDARD</b>	<b>BOARD</b>	<b>SCHOOL</b>	<b>PERCENTAGE AND PASSING YEAR</b>			
	10th	CBSE	ST. PAUL'S SR. SEC. SCHOOL	66.5	(2007)		
	12th	CBSE	ST. PAUL'S SR. SEC. SCHOOL	72	(2010)		
<b>PROFESSIONAL QUALIFICATION</b>	B.Tech (ECE)	GLA UNIVERSITY	GLA UNIVERSITY	63.60	(2015)		
<b>EXPERIENCE/ INTERESTS/ ACHIEVEMENTS</b>	<ol style="list-style-type: none"> <li>1. Having good interpersonal and communication skill.</li> <li>2. Good knowledge in MATHS, REASONING and GENERAL STUDIES.</li> <li>3. Clear UPSC PRELIM 2021, UPPSC PRELIM (2020 and 2022) and SSC CGL 2022.</li> <li>4. Interested in Current Affairs and Contemporary Issues.</li> </ol>						
<b>LANGUAGES KNOWN</b>	1-ModelSim, Xilinx & Cadence Virtuoso. 2-C-Language, C++ and Verilog Language.						
<b>INDUSTRIAL TRAINING</b>	Based on Verilog from Tevatron Technologies pvt. ltd.						
<b>PROJECTS UNDERTAKEN</b>	1- Digital Security System based on Verilog over FPGA. 2- An 180nm Low Noise Amplifier With Single Ended and Differential Output by using Cadence Virtuoso.						
<b>SEMINARS &amp; CONFERENCES / PAPER PRESENTATION</b>	<ul style="list-style-type: none"> <li>• IEEE conference: Attend lecture over Essence of power aware CMOS design and Techniques.</li> <li>• Work as Volunteer in IEEE International conference CICN-2013.</li> <li>• i3indya Technologies: Attend workshop over HACK-O-MANIA. Attend workshop over ROBO-O-MANIA.</li> </ul>						
<b>PERMANENT ADDRESS</b>	H.NO-22, GALI NO-01, GOYAL FARM, TAJPUR ROAD, NEAR STANFORD CONVENT SCHOOL, BADARPUR EXTENSION, DELHI, 110044.		<b>CONTACT NO:</b>	9540911496			
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